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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,837	09/14/2000	Sunil Tomar	501	1616

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EXAMINER
ODLAND, DAVID E

ART UNIT	PAPER NUMBER
2662	18

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,837	TOMAR ET AL.	
	Examiner	Art Unit	
	David Odland	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *17* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 2 and 11 are objected to because of the following informalities:

Claim 2 improperly recites the term 'control' twice in line 3;

Claim 11 recites "...converting the parallel signal multiple serial signals..." the English grammar of this part of the claim language is improper;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,2,11,14,15,18,19,22,23 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Baylock (USPN 4,924,464), hereafter referred to as Baylock.

Referring to claim 1, Baylock discloses an apparatus comprising:

a plurality of transmission circuits to transmit data over one or more of a set of output lines (a plurality of outputs that transmit data over output lines (see claim 1 and figure 6));

a plurality of receiving circuits to receive data over one or more of a set of input lines (a plurality of inputs that receive data over the input lines (see claim 1 and figure 6)); and

a plurality of parallel-serial conversion circuits coupled to the plurality of transmission circuits and to the plurality of receiving circuits (a plurality of parallel-serial conversion coupled to the outputs and inputs (see claim 1 and figure 6)), the plurality of conversion circuits to

convert parallel signals to one or more sets of serial signals and to send the converted serial signals to one or more corresponding transmission circuits (parallel signals are converted into serial signal by the converters and the converted signals are transmitted through the outputs (see claim 1 and figure 6)) and to receive one or more sets of serial signals from one or more of the receiving circuits and to convert the serial signals to parallel signals (serial signals are received and converted to parallel signals by the converters (see claim 1 and figure 6)).

Referring to claim 2, Baylock discloses the system discussed above. Furthermore, Baylock discloses that a control circuit is coupled to the plurality of transmission circuits, to the plurality of receiving circuits and to the plurality of parallel-serial conversion circuits (a control signals, inherently from a controller, are sent to the output circuits, input circuits and conversion circuits to control such elements of the system (see column 4 lines 9-29 and claim 1 and figure 6)), the control circuit to control conversion of signals between parallel and serial formats and to control transmission and receiving of data (the control signals are used to control the receptions, transmissions and conversions of the data (see column 4 lines 9-29 and claim 1 and figure 6)).

Referring to claim 11, Baylock discloses a system comprising receiving a parallel signal at a first rate (a parallel signal is received at a first rate (claim 1));

converting the parallel signal multiple serial signals (the parallel signals are converted into serial signals (see claim 1)); and

transmitting the multiple serial signals at a second rate (the converted signals are transmitted at a particular rate (see claim 1)).

Referring to claim 14, Baylock discloses the system discussed above. Furthermore, Baylock discloses transmitting the multiple serial signals at the second rate with a first

transmitting circuit and with a second transmitting circuit (data from the serial outputs are transmitted at a particular rate by way of a number of transmission circuits (see claim 1 and figure 6)).

Referring to claim 15, Baylock discloses a method comprising the steps of receiving multiple serial signals at a first rate (a plurality of serial signals are received at a first particular rate (see claim 1));

converting the multiple serial signals to a parallel signal (converting of many serial inputs into a parallel output (see claim 1 and figure 6));

transmitting the parallel signal at a second rate (the parallel signal is transmitted at a second particular rate (see claim 1)), wherein the second rate is greater than the first rate (the serial input bit rate may be slower than the parallel output bit rate (see claim 6)).

Referring to claim 18, Baylock discloses the system discussed above. Furthermore, Baylock discloses receiving the multiple serial signals at the first rate with a first receiving circuit and with a second receiving circuit (the serial signals are received at a first particular rate by way of a plurality of receiving circuits (see claim 1 and figure 6)).

Referring to claim 19, Baylock discloses a system comprising:

means for receiving a parallel signal at a first rate (receiving circuits for receiving a parallel signal (see claim 1));

means for converting the parallel signal multiple serial signals (a converter for converting the parallel signal into multiple serial signals (see claim 1)); and

means for transmitting the multiple serial signals at a second rate (the plurality of serial signals are transmitted at a second particular rate (see claim 1)).

Referring to claim 22, Baylock discloses the system discussed above. Furthermore, Baylock discloses means for transmitting the multiple serial signals at the second rate with a first transmitting circuit and with a second transmitting circuit (data from the serial outputs are transmitted at a particular rate by way of a number of transmission circuits (see claim 1 and figure 6)).

Referring to claim 23, Baylock discloses a system comprising:

means for receiving multiple serial signals at a first rate (a receiving circuit for receiving a plurality of serial signals at a first particular rate (see claim 1));

means for converting the multiple serial signals to a parallel signal (a converter for converting the serial signals into a parallel signal (see claim 1));

means for transmitting the parallel signal at a second rate, wherein the second rate is greater than the first rate (transmitting the parallel signal at a rate which can be greater than the first particular rate (see claims 1 and 6)).

Referring to claim 26, Baylock discloses the system discussed above. Furthermore, Baylock discloses receiving the multiple serial signals at the first rate with a first receiving circuit and with a second receiving circuit (the plurality of serial signals are received at the first particular rate by way of a plurality of receiving circuits (see claim1 and figure 6)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-10,12,16,20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baylock.

Referring to claim 3, Baylock discloses the system discussed above. Furthermore, Baylock discloses converting a received parallel signal to a corresponding serial signal at a first data rate (the parallel-serial converter converts the parallel data into serial data at a particular rate (see claim 1 and figure 6)).

Referring to claim 4, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of transmission circuits transmits the converted serial signal at the first data rate (the parallel-serial converters transmit the converted signals at a particular rate (see claim 1 and figure 6)).

Referring to claim 5, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of parallel-serial conversion circuits receives data at a first data rate as a parallel signal (the converters receive parallel signals (see claim 1 and figure 6)) and converts the parallel signals to multiple serial signals (the parallel signals are converted into multiple serial signals (see claim 1 and figure 6)).

Referring to claim 6, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the transmission circuits transmits the multiple serial signals at the second data rate (the output circuits transmit the converted multiple serial signals at a particular rate (see claim 1 and figure 6)).

Referring to claim 7, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of parallel-serial conversion circuits receives a serial

signal at a first data rate (the conversion circuit receives a serial signal at a first particular rate (see claim 1 and figure 6)) and converts the serial signal to a parallel data at the first data rate (the received data is converted into parallel data at the particular rate (see claim 1 and figure 6)).

Referring to claim 8, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of receiving circuits receives the serial signal at the first data rate and sends the serial signal to the parallel serial conversion circuit (the serial data is received at a particular rate and send to the serial-parallel conversion circuit to be converted (see claim1 and figure 6)).

Referring to claim 9, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the plurality of parallel-serial conversion circuits receives multiple serial signals at a first data rate (the conversion circuit receives multiple serial signals at a first particular rate (see claim 1 and figure 6)) and converts the serial signals to parallel data at a second data rate (the serial signals are converted at a second particular rate (see claim 1 and figure 6)), where the second data rate is greater than the first data rate (transmitting the parallel signal at a second rate which can be greater than the first particular rate (see claim 1 and claim 6)).

Referring to claim 10, Baylock discloses the system discussed above. Furthermore, Baylock discloses that one of the receive circuits receives the multiple serial signals at the first data rate (multiple inputs circuits receive serial data at a particular rate (see claim 1 and figure 6)).

Referring to claims 3, 5, 7, 9, 12, 16, 20, 24 Baylock discloses the system discussed above. Baylock does not disclose that the parallel signal is SONET framed data. However, SONET is a

well known established communications protocol. Therefore, it would have been obvious to one skilled in the art at the time of the invention to use the system of Baylock with SONET data because it would save developmental costs using an already well-known, existing protocol rather than devising an entirely new protocol.

6. Claims 13,17,21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baylock in view of Upp et al. (USPN 5,040,170), hereafter referred to as Upp.

Referring to claims 13,17,21 and 25 Baylock discloses the system discussed above. Baylock does not disclose performing stuffing such that the sum of a number of multiple signals at the second rate times the second rate is equal to the first rate. However, Upp discloses a system where bit stuffing is performed in the creation of SONET signals (see column 7 lines 61-68 and column 8 lines 1-6) and a parallel STS-3 SONET signal is converted to multiple serial SONET STS-1 signals (see column 6 lines 38-46 and figure 1). It would have been obvious to one skilled in the art at the time of the invention to perform, in the system of Baylock, stuffing operations such that the sum of a number of multiple signals at the second rate times the second rate is equal to the first rate because so would allow proper timing to be maintained between the inputs and outputs in instances where the output rate is greater than the input rate.

Conclusion

7. The following prior art, which is made of record and not relied upon, is considered pertinent to applicant's disclosure:

a. U.S. Patent Number 4637012 to Crabbe Jr.

b. U.S. Patent Number 4717914 to Scott.

c. U.S. Patent Number 5805088 to Butter et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

April 29, 2003

JOHN PEZZLO
PRIMARY EXAMINER